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The undersigned hereby certifies that I am conversant in both Japanese and English languages, that I have prepared the attached English translation of the first draft patent application, Exhibit A, and that the English translation is a true, faithful and accurate translation of Exhibit A.

I further declare that all statements made of my own knowledge are true and that all statements made on information and belief are with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under 18 USC § 1001, and that

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Request to Check a Specification to be filed

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Title of the Invention: Method of testing mask pattern and a mask

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[Comments]

Please supplement the paragraph [0039]

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[Name of Attachment]	Specification	1
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[Name of Attachment]	Abstract	1

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[Title of Document] Specification

[Title of the Invention] Method of testing mask pattern, program for testing mask pattern, and method of fabricating mask

[Claims]

[Claim 1] A method of testing a mask pattern, comprising:

preparing a mask design pattern to be tested, as a pattern designed as a mask layer to be tested;

applying optical proximity-effect compensation to said mask design pattern to be tested to thereby form a mask pattern of said mask layer;

preparing another mask design pattern as a pattern designed as another mask layer;

dividing said mask design pattern to be tested into a plurality of areas in accordance with said another mask design pattern;

determining sampling points on a pattern edge of said mask design pattern to be tested;

determining a test standard for each of said areas;

simulating a resist pattern to be formed on a resist by exposing said resist to a light through a mask having said mask pattern; and

testing said mask pattern by checking whether a dimensional gap between said mask design pattern to be tested and said resist pattern at each of said sampling points is within a test standard associated with an area to which each of said sampling points belongs,

wherein said test standard for a first area among said areas and said test standard for a second area among said areas are different from each other.

[Claim 2] The method as set forth in claim 1, wherein a first sampling point located in said first area, among said sampling points, is determined in accordance with a first process, and a second sampling point located in said second area, among said sampling points, is determined in accordance with a

second process different from said first sampling process.

[Claim 3] The method as set forth in claim 1, further comprising dividing a pattern edge of said mask design pattern to be tested into a plurality of portions, wherein said test standard is determined for each of said portions.

[Claim 4] The method as set forth in claim 1, wherein said mask design pattern to be tested is a pattern for forming a wiring layer, said another mask design pattern is a pattern for forming a contact reaching said wiring layer, and said first area includes a contact-associated area including a contact area in which said contact makes contact with said wiring layer.

[Claim 5] The method as set forth in claim 4, wherein said contact-associated area is comprised of said contact area and an ambient area surrounding said contact area.

[Claim 6] The method as set forth in claim 1, wherein said mask design pattern to be tested is a pattern for forming a wiring layer including a gate of a MOS transistor, said another mask design pattern is a pattern for forming an active area of said MOS transistor, and said first area includes a field-layer-associated area including an active-area-projecting area obtained by projecting said active area onto said mask design pattern to be tested.

[Claim 7] The method as set forth in claim 6, wherein said field-layer-associated area is comprised of said active-area-projecting area and an ambient area surrounding said active-area-projecting area.

[Claim 8] A program for causing a computer to carry out a method of testing a mask pattern, steps executed by said computer in accordance with said program including:

preparing a mask design pattern to be tested, as a pattern designed as a mask layer to be tested;

applying optical proximity-effect compensation to said mask design pattern to be tested to thereby form a mask pattern of said mask layer;

preparing another mask design pattern as a pattern designed as another

mask layer;

dividing said mask design pattern to be tested into a plurality of areas in accordance with said another mask design pattern;

determining sampling points on a pattern edge of said mask design pattern to be tested;

determining a test standard for each of said areas;

simulating a resist pattern to be formed on a resist by exposing said resist to a light through a mask having said mask pattern; and

testing said mask pattern by checking whether a dimensional gap between said mask design pattern to be tested and said resist pattern at each of said sampling points is within a test standard associated with an area to which each of said sampling points belongs,

wherein said test standard for a first area among said areas and said test standard for a second area among said areas are different from each other.

[Claim 9] A method of forming a mask, comprising:

carrying out the method of testing a mask pattern, set forth in any one of claims 1 to 7; and

transferring said mask pattern to a mask.

[Detailed Description of the Invention]

[0001]

[Field of the Invention]

The invention relates to a method of testing a mask pattern, and a program for testing a mask pattern, and more particularly to a method of testing whether a mask pattern which is formed by applying optical proximity-effect compensation can be a base to form a desired resist pattern.

[0002]

[Prior Art]

Recent reduction in a design-rule of a semiconductor device causes a problem of optical proximity effect. Herein, optical proximity effect is defined as

phenomenon in which a pattern different in shape from a mask pattern formed in a mask is formed on a resist. For instance, when a resist is exposed to a light through a mask having an L-shaped pattern, corners of an L-shaped pattern formed in a resist are rounded due to optical proximity effect. In addition, a width of a line pattern formed on a resist is dependent on an interval between line patterns due to optical proximity effect. For instance, a line pattern among line patterns formed in a high density, and a line pattern solitarily formed would have widths different from each other on a resist, even if they had a common width on a mask.

[0003]

In order to compensate for optical proximity effect, optical proximity-effect compensation (OPC) is carried out during a fabrication process of a mask pattern. That is, a desired resist pattern is modified (namely, optical proximity-effect compensation is applied), taking optical interference into consideration, to thereby form a mask pattern. A resist pattern is transferred to a resist through a mask having the thus formed mask pattern. The thus formed mask pattern is different in shape from the desired resist pattern.

[0004]

The optical proximity-effect compensation ensures a desired resist pattern, but causes necessity of testing a mask pattern by virtue of computer simulation. A shape of a resist pattern transferred from a mask having a certain mask pattern is dependent on interference of a light passing through the mask pattern. Definition of a resist pattern with such interference being taken into consideration cannot be accomplished without computer simulation. Hence, whether it is possible to form a desired resist pattern, based on a mask having a certain mask pattern, is tested by computer simulation.

[0005]

In testing a mask pattern, it is important to be able to surely detect a non-desired resist pattern. The patent reference 1 has suggested a method of

detecting deformation of a pattern located remote from an edge of a pattern (that is, detecting a resist pattern at a location where a resist pattern should not be formed, if a resist pattern is formed accurately in accordance with a designed pattern). The suggested method includes the steps of determining sampling points (points at which a test is carried out) in a predetermined area other than an edge of a designed pattern, and comparing a dimension of a designed pattern with a dimension of a resist pattern calculated by simulation, at each of the sampling points. The suggested method makes it possible to detect deformation of a pattern in an area remote from an edge of a designed pattern, by selectively determining sampling points in a predetermined area other than an edge of a designed pattern.

[0006]

It is preferable in a test of a mask pattern to determine a test standard, taking into consideration a structure of a semiconductor integrated circuit as a final product. Herein, a test standard is a standard in accordance with which a mask pattern is judged as to whether it is accurately formed. A decision as to whether a mask pattern is accurate is dependent on whether a resist pattern by which a semiconductor integrated circuit as a final product can properly operate is formed. Accordingly, a test standard is determined so as to make it possible to form a resist pattern by a semiconductor integrated circuit as a final product can properly operate.

[0007]

When severe restriction is applied to a dimension of a resist pattern for properly operating a semiconductor integrated circuit, a test standard used for testing a mask pattern has to be determined accordingly. For instance, a width of a gate line in a MOS transistor much exerts an influence on characteristics of a MOS transistor. Accordingly, a width of a gate line has to be accurately controlled, and hence, a test standard used for testing a width of a resist pattern used as a mask through which a gate line is etched has to be determined

accordingly. Furthermore, when a contact (or a via) is designed to make contact with a wiring layer, the wiring layer has to be accurately positioned in order to ensure for the contact to make contact with the wiring layer, and hence, a position of a resist pattern used as a mask through which a wiring layer is etched has to be determined accordingly.

[0008]

To the contrary, when a resist pattern has a broad dimensional margin in which a semiconductor integrated circuit can properly operate, it is not necessary to determine a sever test standard. This is because a sever test standard causes an increase in repair of a mask pattern with the result of an increase in TAT for fabricating a mask.

[0009]

In addition, it is necessary to select sampling points at appropriate locations in testing a mask pattern, taking a structure of a semiconductor integrated circuit as a final product into consideration. In order to thoroughly test a mask pattern for surely detecting a non-desired resist pattern, it is effective to test a mask pattern with a lot of sampling points. However, a lot of sampling points would increase calculation necessary for carrying out simulation, resulting in that simulation takes much time. Accordingly, it is preferable that sampling points are selected only at appropriate locations, and a mask pattern is tested with a small number of sampling points. As mentioned earlier, a semiconductor integrated circuit has portions in which a dimension of a pattern has to be accurately controlled, and portions in which it is not always necessary to accurately control a dimension of a pattern. Hence, it is preferable that a lot of sampling points are selected for the former portions, and a small number of sampling points are selected for the latter portions for making it possible to accurately test a mask pattern with a small number of sampling points.

[0010]

[Patent reference 1]

[0011]

[Problems to be solved by the Invention]

It is an object of the present invention to provide a method of testing a mask pattern, based on a test standard determined in accordance with a structure of a semiconductor integrated circuit as a final product.

It is another object of the present invention to provide a method of testing a mask pattern, in which sampling points used for testing a mask pattern are selected in accordance with a structure of a semiconductor integrated circuit as a final product, ensuring that a mask pattern is accurately tested with a small number of sampling points.

[0012]

[Solution to the Problems]

Hereinbelow is described the solution to the problems through the use of reference numerals used in later described embodiments. The reference numerals are indicated only for the purpose of clearly showing correspondence between claims and the embodiments. It should be noted that the reference numerals are not allowed to use in the interpretation of claims of the present application.

[0013]

The present invention provides a method of testing a mask pattern, including:

preparing a mask design pattern (11) to be tested, as a pattern designed as a mask layer to be tested,

applying optical proximity-effect compensation to the mask design pattern (11) to be tested to thereby form a mask pattern of the mask layer,

preparing another mask design pattern as a pattern designed as another mask layer,

dividing the mask design pattern (11) to be tested into a plurality of areas

(21, 22, 23) in accordance with the another mask design pattern,

determining sampling points (15'-17') on a pattern edge of the mask design pattern (11) to be tested,

determining a test standard for each of the areas (21-23),

simulating a resist pattern to be formed on a resist by exposing the resist to a light through a mask having the mask pattern, and

testing the mask pattern by checking whether a dimensional gap between the mask design pattern (11) to be tested and the resist pattern at each of the sampling points (15'-17') is within a test standard associated with an area to which each of the sampling points belongs,

wherein the test standard for a first area (21, 22) among the areas (21, 22, 23) and the test standard for a second area (23) among the areas are different from each other.

[0014]

In accordance with the above-mentioned method, a mask design pattern (10) is divided into a plurality of areas, and a test standard is determined for each of the areas. By dividing the mask design pattern (10) into a plurality of areas through the use of a pattern of another mask structurally relating to a mask to be tested, the method makes it possible to test a mask pattern with an appropriate test standard determined in accordance with a structure of a semiconductor integrated circuit as a final product.

[0015]

A first sampling point (15'-17') located in the first area (21, 22), among the sampling points (15'-17'), may be determined in accordance with a first process, and a second sampling point (17') located in the second area (23), among the sampling points (15'-17'), may be determined in accordance with a second process different from the first sampling process. Thus, it is possible to select sampling points (15'-17') at appropriate locations in accordance with a structure of a semiconductor integrated circuit as a final product.

[0016]

The method may further include dividing a pattern edge of the mask design pattern (11) to be tested into a plurality of portions, wherein it is preferable that a test standard for a first portion among the portions and a test standard for a second portion among the portions are different from each other.

[0017]

It is preferable that the mask design pattern (11) to be tested is a pattern for forming a wiring layer, the another mask design pattern is a pattern for forming a contact reaching the wiring layer, and the first area (21, 22) includes a contact-associated area (21) including a contact area (21a) in which the contact makes contact with the wiring layer. In such a case, it is preferable that the contact-associated area (21) is comprised of the contact area (21a) and an ambient area (21b) surrounding the contact area (21a).

[0018]

It is preferable that the mask design pattern (11) to be tested is a pattern for forming a wiring layer including a gate of a MOS transistor, the another mask design pattern is a pattern for forming an active area of the MOS transistor, and the first area (21, 22) includes a field-layer-associated area (22) including an active-area-projecting area (22a) obtained by projecting the active area onto the mask design pattern (11) to be tested, in which case, it is preferable that the field-layer-associated area (22) is comprised of the active-area-projecting area (22a) and an ambient area (22b) surrounding the active-area-projecting area (22a).

[0019]

The present invention provides a program for causing a computer (1) to carry out a method of testing a mask pattern, steps executed by the computer in accordance with the program including:

preparing a mask design pattern (11) to be tested, as a pattern designed as a mask layer to be tested,

applying optical proximity-effect compensation to the mask design pattern (11) to be tested to thereby form a mask pattern of the mask layer,

preparing another mask design pattern as a pattern designed as another mask layer,

dividing the mask design pattern (11) to be tested into a plurality of areas (21-23) in accordance with the another mask design pattern,

determining sampling points (15'-17') on a pattern edge of the mask design pattern (11) to be tested,

determining a test standard,

simulating a resist pattern to be formed on a resist by exposing the resist to a light through a mask having the mask pattern, and

testing the mask pattern by checking whether a dimensional gap between the mask design pattern (11) to be tested and the resist pattern at each of the sampling points (15'-17') is within a test standard associated with an area to which each of the sampling points (15'-17') belongs,

wherein the test standard for a first area (21, 22) among the areas (21-23) and the test standard for a second area (23) among the areas are different from each other.

[0020]

[Embodiments in accordance with the Invention]

A method of testing a mask pattern in accordance with an embodiment of the present invention is explained hereinbelow with reference to drawings.

[0021]

FIG. 2 is a block diagram of a computer system 1 which puts a method of testing a mask pattern in accordance with an embodiment the present invention into practice. The computer system 1 is comprised of an input device 2, a communication unit 3, a memory 4, a CPU 5, and an output device 6. The input device 2 acts as a man-machine interface between a user and the computer system 1. For instance, the input device 2 is comprised of a keyboard or a

mouse.

[0022]

The communication unit 3 receives a pattern designed by means of CAD (Computer Aided Design) from an external unit through a network (not illustrated). The designed pattern is defined as a target pattern of a resist pattern to be formed on a resist.

[0023]

The memory 4 stores therein a program and data both necessary for carrying out a method of testing a mask pattern in accordance with an embodiment of the present invention. Specifically, the memory 4 sores therein an OPC tool 4a, a tool 4b for testing a mask pattern, and a main program 4c. Herein, the OPC tool 4a is a program used for applying optical proximity-effect compensation to the designed pattern to thereby fabricate a mask pattern to be transferred onto a mask. The mask-pattern testing tool 4b is a program used for testing whether a desired resist pattern is formed onto a resist when the resist is exposed to a light through the mask having the thus fabricated mask pattern. The mask-pattern testing tool 4b carries out lithography simulation to a mask pattern of a mask layer to be tested, to thereby simulate a resist pattern to be transferred onto a resist. Furthermore, the mask-pattern testing tool 4b judges whether a dimensional gap between the designed pattern having been received through the communication unit 3 and a resist pattern having been calculated by simulation is within a test standard. In the specification, a dimension of a pattern means an interval between the pattern and patterns located adjacent thereto, a width of the pattern, and a location of the pattern. In the main program 4c are written steps for carrying out a method of testing a mask pattern in accordance with the present embodiment. Specifically, the steps shown in FIG. 1, a flow chart, are written in the main program 4c.

[0024]

The memory 4 further includes a data area 4d to store therein data

necessary for carrying out a method of testing a mask pattern in accordance with the present embodiment. The data area 4d stores data necessary for carrying out a method of testing a mask pattern in accordance with the present embodiment, such as a designed pattern received through the communication unit 3, a mask pattern fabricated by the OPC tool 4a, and a resist pattern fabricated by simulation.

[0025]

The CPU 5 executes the OPC tool 4a, the mask-pattern testing tool 4b and the main program 4c to carry out steps necessary for testing a mask pattern.

[0026]

The output device 6 is comprised of a CRT (cathode ray tube) display and a printer, for instance. The output device 6 displays results of testing a mask pattern, and prints out the results.

[0027]

FIG. 1 is a flow chart showing steps to be carried out in a method of testing a mask pattern in accordance with the present embodiment. In the present embodiment, a mask pattern to be transferred to a mask used for forming a wiring layer (gate layer) of a MOS transistor is tested. First, the computer system 1 receives a pattern designed (step S01). In step S01, the computer system 1 receives not only the designed pattern of a mask layer to be tested, but also a designed pattern of a mask layer structurally concerning the mask layer to be tested. Specifically, since the mask layer to be tested is comprised of a gate layer in the present embodiment, the computer system 1 receives not only a designed pattern of a gate layer, but also designed patterns of a field layer for defining an active region and a contact layer for forming a contact reaching a wiring in the gate layer. As mentioned later, designed patterns of mask layers structurally relating to the mask layer to be tested are used for dividing a designed pattern of the mask layer into a plurality of areas.

[0028]

Then, optical proximity-effect compensation (OPC) is applied to the designed pattern of the mask layer to be tested, to thereby form a mask pattern (step S02). The optical proximity-effect compensation is carried out by the OPC tool 4a. In the subsequent steps, the mask pattern formed in step S02 is tested. If it is judged that a desired resist pattern can be formed based on the mask pattern tested, the mask pattern is transferred to a mask. Thus, there is formed a mask.

[0029]

Then, an edge of the designed pattern (a side of the designed pattern) of the mask layer to be tested is divided into a plurality of portions (step S03). As illustrated in FIG. 3, a pattern edge of the designed pattern 11 of the mask to be tested is divided into three portions, that is, line end portions 12, corner portions 13, and a remainder portion 14. The line end portion 12 is defined as a portion of a line extending in a direction which portion is defined by two lines extending perpendicularly to the direction. The line end portion 12 has a width smaller than a predetermined width. The corner portion 13 is defined as a portion extending from corners in a rectangular area constituting the designed pattern 11, having a length equal to or smaller than a predetermined length L, and not overlapping the line end portion 12. Furthermore, the corner portion 13 is defined as a portion other than a portion in which the rectangular areas makes contact with each other. The remainder portion 14 is defined as a portion except the line end portions 12 and the corner portions 13 in a pattern edge of the designed pattern 11.

[0030]

Then, as illustrated in FIG. 1, sampling candidate points are selected on a pattern edge of the designed pattern of the mask layer to be tested (step S04). As mentioned later, some of the thus selected sampling candidate points are determined as sampling points at which a mask pattern is tested.

[0031]

The sampling candidate points are selected differently in accordance with the portions of the pattern edge. A sampling candidate point 15 is selected at a center of a side of the designed patterns 11 in the end portion 12. In the corner portions 13, sampling candidate points 16 are selected at a predetermined interval starting from each of the corners of the designed pattern 11. The sampling candidate point 16 is not selected at the corners of the designed pattern 11. In the remainder portion 14, sampling candidate points 17 are selected at a center of side of the designed pattern. By selecting sampling candidate points in the above-mentioned manner, it is possible to select a lot of sampling candidate points (and sampling points) in both the line end portion 12 and the corner portions 13 both of which are much influenced by optical proximity effect.

[0032]

Then, the designed pattern of the mask layer to be tested is divided into a plurality of areas (step S05). As illustrated in FIG. 4, the designed pattern 11 of a gate layer as the mask layer to be tested is divided into contact-associated areas 21, a field-layer-associated area 22 and a remainder area 23. Each of the contact-associated areas 21 is comprised of a projecting area 21a formed by projecting a contact reaching a wiring in a gate layer, onto the designed pattern 11 of the gate layer, and an ambient area 21b surrounding the projecting area 21a and having a width, measured from an outer edge of the projecting area 21a, equal to or smaller than M1. The field-layer-associated area 22 is comprised of a projecting area 22a formed by projecting an active area of a MOS transistor onto the designed pattern 11 of the gate layer, and an ambient area 22b surrounding the projecting area 22a and having a width, measured from an outer edge of the projecting area 22a, equal to or smaller than M2. The remainder area 23 is an area other than the contact-associated areas 21 and the field-layer-associated area 22 in the designed pattern 11 of the gate layer.

[0033]

Then, sampling points are selected (step S06). As illustrated in FIG. 5, a part of the sampling candidate points 15, 16 and 17 having been selected in the line end portion, the corner portions, and the remainder portion in step S04, respectively, is selected as sampling points. The sampling points selected among the sampling candidate points 15, 16 and 17 are illustrated as the sampling points 15', 16' and 17', respectively.

[0034]

The sampling points are selected in different manners in accordance with the areas into which the designed pattern are divided. Specifically, the sampling points are selected in different manners in accordance with the contact-associated areas 21, the field-layer-associated area 22, and the remainder area 23. As illustrated in FIG. 5, all of the sampling candidate points 15, 16 and 17 having been selected in the contact-associated areas 21 and the field-layer-associated area 22 are selected as the sampling points 15', 16' and 17'. In contrast, in the remainder area 23, only the sampling candidate points 17 having been selected in the remainder portion are selected as the sampling points 17'.

[0035]

By selecting the sampling points in the above-mentioned manner, it is possible to appropriately select the sampling points in accordance with a structure of a semiconductor integrated circuit as a final product. For instance, dimensions of an area in which a contact makes contact with a wiring formed in a gate wiring layer, and an area around the area (namely, the contact-associated area 21) have to be accurately tested in order to ensure electrical connection in a semiconductor integrated circuit. Furthermore, in order to have a MOS transistor in a semiconductor integrated circuit accomplished desired performances, dimensions of a portion acting as a gate of a MOS transistor and an area around the portion (namely, the field-layer-associated area 22) have to be accurately tested. On the other hand, the rest of the designed pattern of a gate

layer does not exert a much influence on behavior of a semiconductor integrated circuit, and hence, it is not necessary to accurately test the rest of the designed pattern of a gate layer. In the present embodiment, since a relatively great number of the sampling points (that is, the sampling points 15', 16' and 17') is selected in the contact-associated area 21 and the field-layer-associated area 22, dimensions in the contact-associated area 21 and the field-layer-associated area 22 are accurately tested, whereas since a relatively small number of the sampling points (that is, the sampling points 17') is selected in the remainder area 23, dimensions in the remainder area 23 are not accurately tested.

[0036]

Then, the mask pattern is tested at each of the sampling points (step S07). A resist pattern to be transferred to a resist when the resist is exposed to a light through a mask to which the mask pattern fabricated in step S02 is transferred is calculated by lithography simulation. The lithography simulation is carried out by the mask-pattern testing tool 4b. Then, there is calculated a gap between dimensions of the designed pattern (namely, a width of a pattern, a space between adjacent patterns and a location of a pattern edge) and dimensions of the resultant resist pattern. If a dimensional gap at a certain sampling point is without a test standard, the sampling point is judged as a sampling point having an error. All of the sampling points are tested as to whether they have an error, and then, the output device 6 outputs a report indicating which sampling points have an error.

[0037]

Test standards used for testing the mask pattern are different from one another in each of the areas of the designed pattern, and are prepared for each of the areas of edges of the designed pattern. For instance, a test standard associated with the sampling points located in the contact-associated area 21, a test standard associated with the sampling points located in the field-layer-associated area 22, and a test standard associated with the sampling

points located in the remainder area 23 are different from one another. In addition, a test standard associated with the sampling points located in the line end portion 12, a test standard associated with the sampling points located in the corner portions 13, and a test standard associated with the sampling points located in the remainder portion 14 are different from one another.

[0038]

By determining test standards in accordance with each of the areas, it would be possible to test a mask pattern with an appropriate test standard determined in accordance with a structure of a semiconductor integrated circuit as a final product. For instance, in the contact-associated area 21 in which a contact (or a via) is designed to make contact with a wiring of a gate layer, a location of a pattern edge of the wiring has to be accurately controlled in order to ensure that the contact makes contact with the wiring. Hence, there is determined a relatively severe test standard with respect to a pattern edge in the contact-associated area 21. In contrast, a location of a pattern edge is not always necessary to be so accurately controlled in the remainder area 23 as the contact-associated area 21. Accordingly, there is determined a relatively loose test standard with respect to a pattern edge in the remainder area 23, avoiding that a test error is unnecessarily detected.

[0039]

Furthermore, by preparing test standards different in accordance with the portions of a pattern edge of the designed pattern,

(You are requested to supplement technical meaning in "different test standards are determined in accordance with a shape of a pattern".)

[0040]

When a test error is detected, a portion of a mask pattern located in the vicinity of a location corresponding to the sampling point at which a test error was found is modified in shape by the OPC tool 4a. The thus modified mask pattern is tested again.

[0041]

When a test error is not detected, the mask pattern is transferred to a mask. Thus, a mask is completely fabricated. A mask pattern is transferred to a mask in a conventional way, and hence, the detail is not explained.

[0042]

In accordance with the above-mentioned embodiment, a test standard used for testing a mask pattern is determined for each of the areas of the designed pattern. Hence, a mask pattern is tested through the use a test standard appropriately determined in accordance with a structure of a semiconductor integrated circuit as a final product.

[0043]

In addition, sampling points are selected in accordance with different processes from one another in association with the areas of the designed pattern. Hence, sampling points are selected at appropriate locations in accordance with a structure of a semiconductor integrated circuit as a final product, and it is ensured that a mask pattern is accurately tested with a small number of sampling points.

[0044]

[Advantages provided by the Invention]

In accordance with the present invention, there is provided a mask pattern test which makes it possible to test a mask pattern through the use of a test standard appropriately determined in accordance with a structure of a semiconductor integrated circuit as a final product.

In addition, sampling points are selected at appropriate locations in accordance with a structure of a semiconductor integrated circuit as a final product, and it is ensured that a mask pattern is accurately tested with a small number of sampling points.

[Brief Description of the Drawings]

[FIG. 1]

FIG. 1 is a flow chart of a method of testing a mask pattern in accordance with an embodiment of the present invention.

[FIG. 2]

FIG. 2 illustrates a computer system 1 in which a method of testing a mask pattern in accordance with the present invention is put into practice.

[FIG. 3]

FIG. 3 illustrates the line end portion 12, the corner portion 13 and the remainder portion 14, and further, the sampling candidate points 15, 16 and 17 selected in those portions.

an end portion of a designed pattern.

[FIG. 4]

FIG. 4 illustrates the contact-associated area 21, the field-layer-associated area 22, and the remainder area 23.

[FIG. 5]

FIG. 5 illustrates the sampling points 15', 16' and 17'.

[Indication by Reference Numerals]

1: Computer system

2: Input device

3: Communication unit

4: Memory

4a: OPC tool

4b: Mask-pattern testing tool

4c: Main program

4d: Data area

5: CPU

6: Output device

11: Designed pattern

12: Line end portion

13: Corner portion

14: Remainder portion

15-17: Sampling candidate points

15'-17': Sampling points

21: Contact-associated area

21a, 22a: Projecting areas

21b, 22b: Ambient areas

[Title of Document] Abstract

[Abstract]

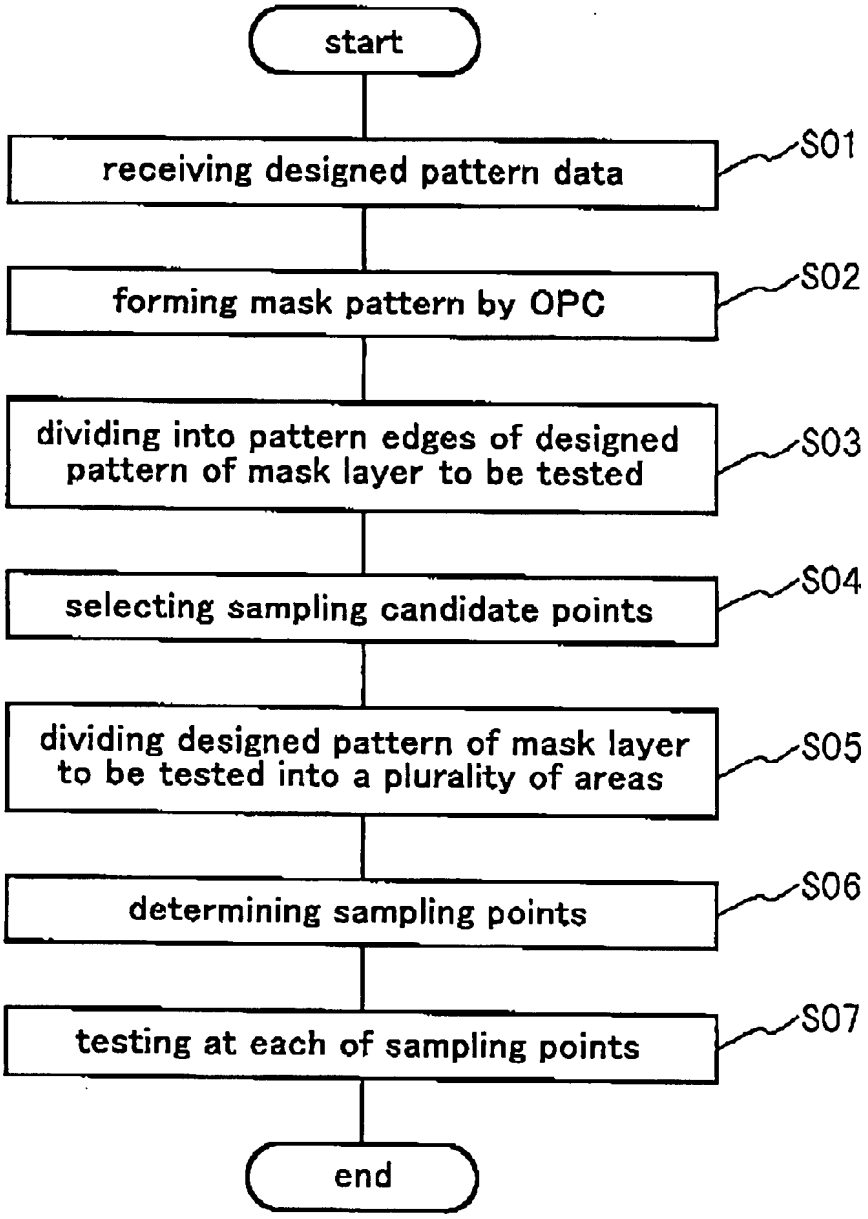
[Object] A method of testing a mask pattern, based on a test standard determined in accordance with a structure of a semiconductor integrated circuit as a final product is provided.

[Solution] The present invention provides a method of testing a mask pattern, including preparing a mask design pattern (11) to be tested, as a pattern designed as a mask layer to be tested, applying optical proximity-effect compensation to the mask design pattern (11) to be tested to thereby form a mask pattern of the mask layer, preparing another mask design pattern as a pattern designed as another mask layer, dividing the mask design pattern (11) to be tested into a plurality of areas (21, 22, 23) in accordance with the another mask design pattern, determining sampling points (15'-17') on a pattern edge of the mask design pattern (11) to be tested, determining a test standard for each of the areas (21-23), simulating a resist pattern to be formed on a resist by exposing the resist to a light through a mask having the mask pattern, and testing the mask pattern by checking whether a dimensional gap between the mask design pattern (11) to be tested and the resist pattern at each of the sampling points (15'-17') is within a test standard associated with an area to which each of the sampling points belongs. The test standard for a first area (21, 22) among the areas (21, 22, 23) and the test standard for a second area (23) among the areas are different from each other.

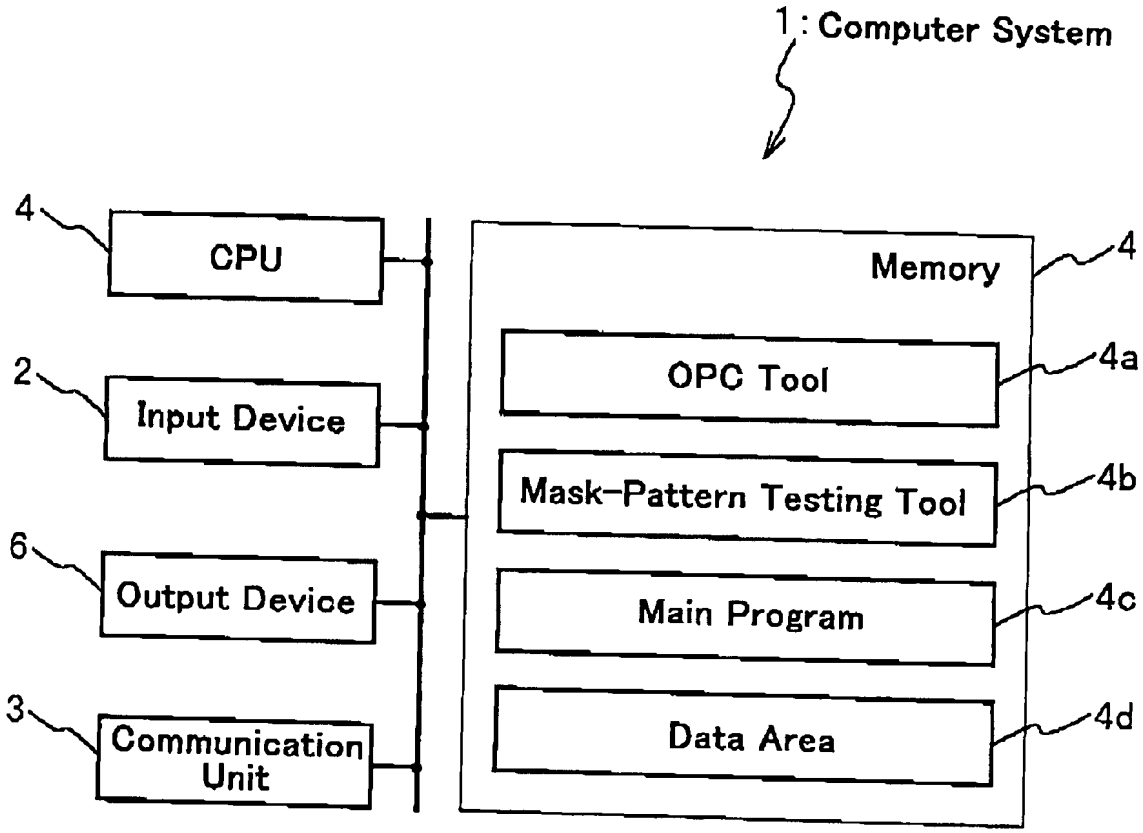
[Drawing to be published] FIG. 1

【Title of Document】 Drawings

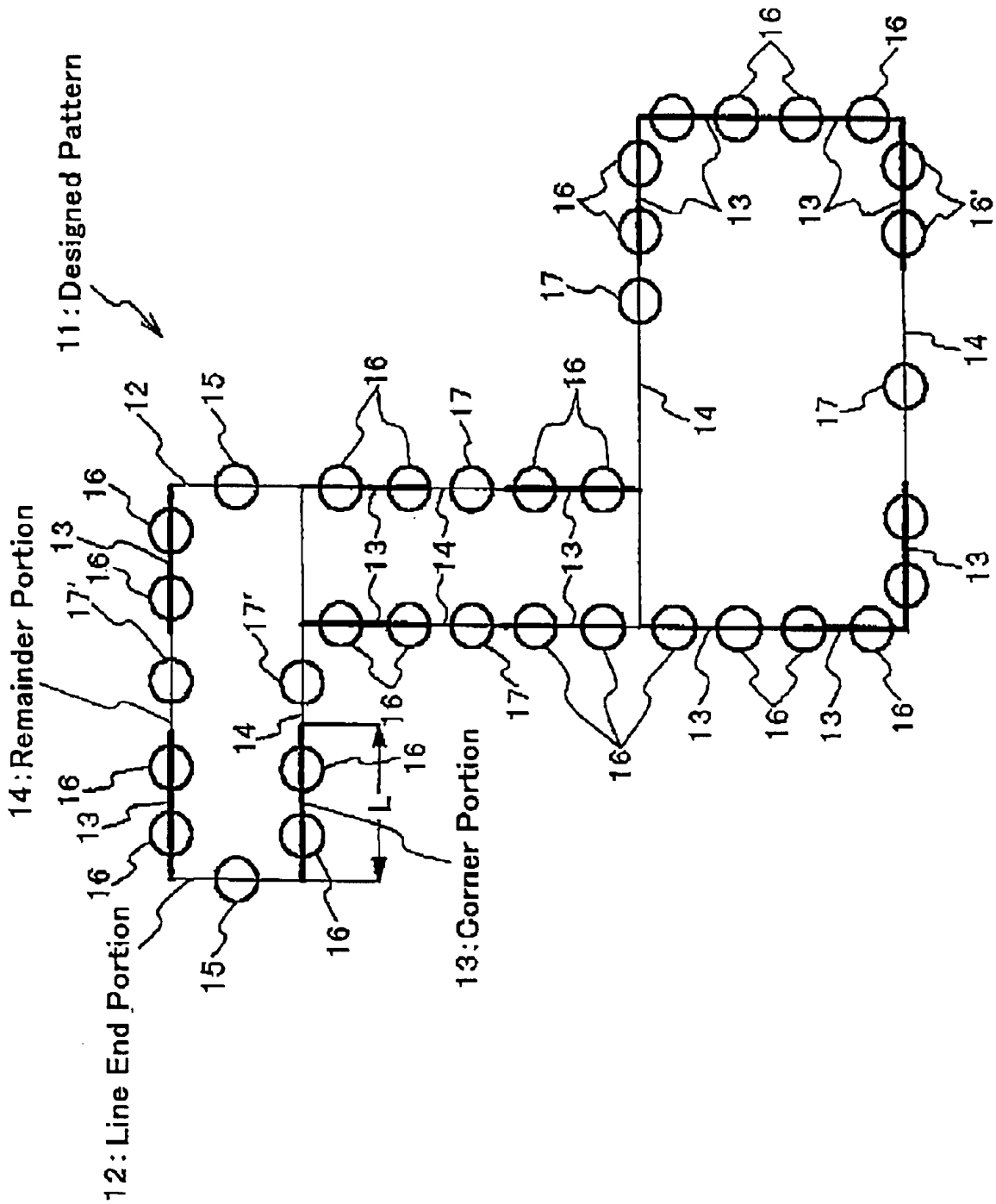
【Fig.1】



【Fig.2】


1 : Computer System
4
CPU
2
Input Device
6
Output Device
3
Communication Unit
Memory
4
OPC Tool
4a
Mask-Pattern Testing Tool
4b
Main Program
4c
Data Area
4d

【Fig.3】


11:Designed Pattern
14:Remainder Portion
12:Line End Portion
13:Corner Portion
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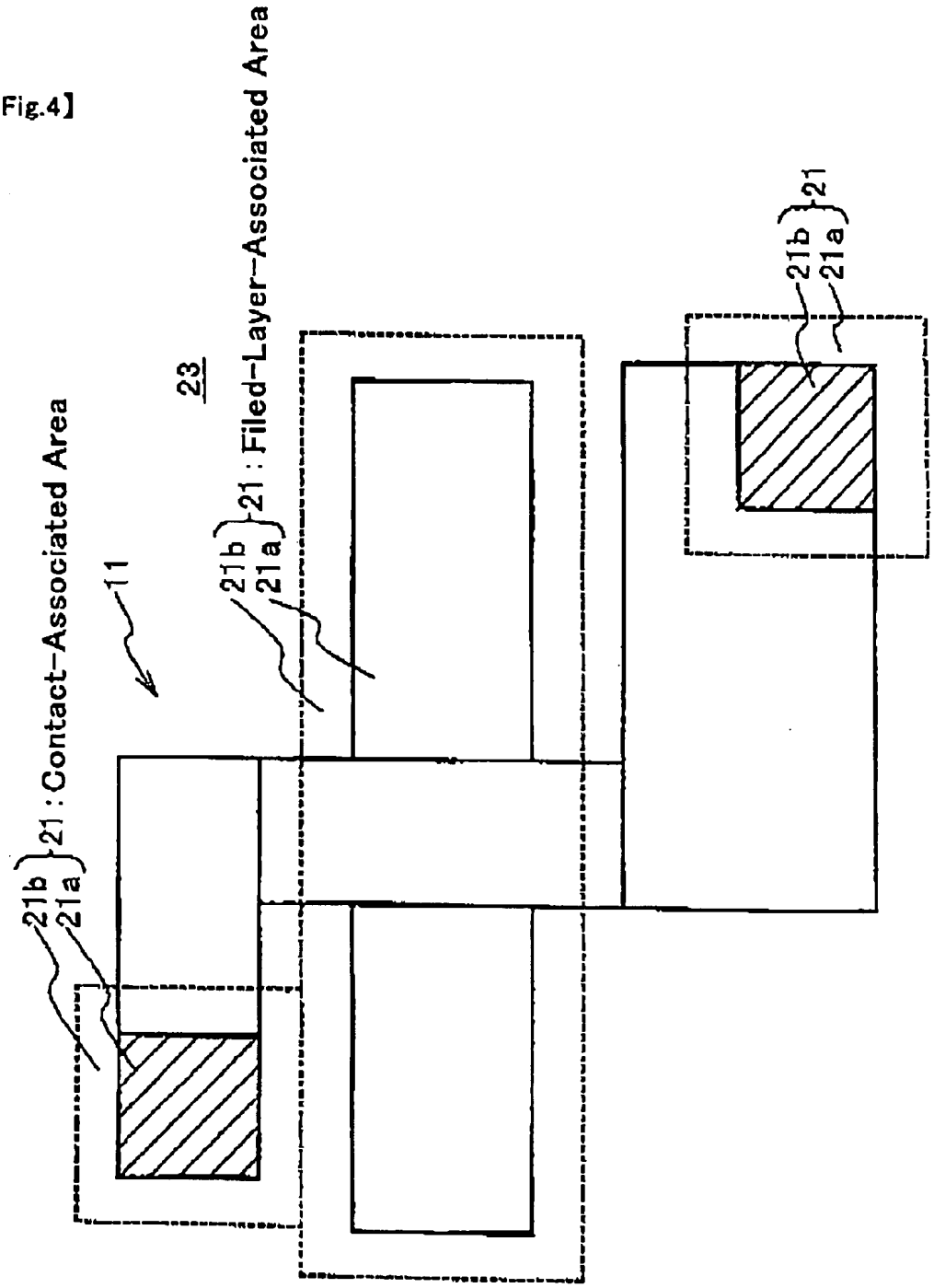
【Fig.4】


23
11
21 : Contact-Associated Area
21 : Filed-Layer-Associated Area
21
21b
21a

【Fig.5】